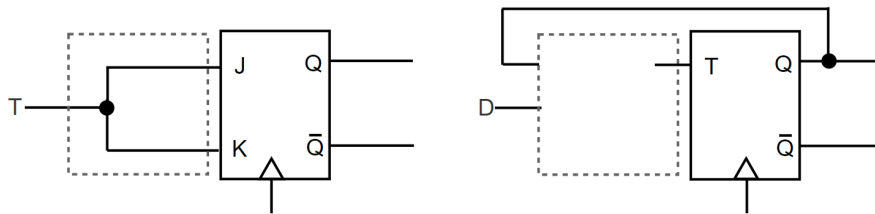


1. Examples handout questions 10 through 19
2. Consider the following circuit:

$$F(A, B, C, D) = ABD + \overline{BC}D + \overline{AC}$$
 - (a) What input transitions could potentially produce a hazard?
 - (b) Give an alternative circuit with the same output as F that does not have any hazards.
 - (c) Give a minimal product-of-sums implementation of F and explain whether there are or are not any static hazards.
3. What is c_5 , the boolean formula for the fifth carry-out bit using the fast-carry scheme described in the lecture notes? How do the number of gate delays required to compute c_5 compare to the number of gate delays required for c_4 (hint: consider the *most* optimal way of parallelising the c_4 and c_5 computations)?
4. Using a 1-of-8 decoder and OR gates create a circuit that takes a 3-bit number $A_2A_1A_0$ and outputs the number of 1's in the input as a 2-bit number Z_1Z_0 .
5. Page 86 of the lecture notes explains that a T flip-flop is essentially a J-K flip-flop with its inputs tied together (e.g., the diagram below, on the left).



It is possible to do something similar to implement a D flip-flop, starting with a T flip-flop. Determine the logic that needs to go in the dotted box for the overall circuit to behave like a D flip-flop. *Hint: The circuit inside the box will need to use Q , the output of the T flip-flop.*

6. Draw a state machine that takes in a sequence of bits at its input IN and outputs 1 if the number of 1's it has seen is even, 0 otherwise. Also, if the machine ever encounters the bit sequence 1001, it should output 0 regardless of the input. You don't need to actually implement the logic for this state machine (just drawing state machine diagram is sufficient).

7. Design a 3 flip-flop counter that transitions through states $Q_2Q_1Q_0 = 000, 100, 110, 111, 011, 001$ and then repeats.